WHAT IS CLAIMED IS:

1. A semiconductor memory comprising:

a memory cell array including a plurality of memory cell rows and at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, and the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction;

a redundancy repair signal generator for generating a redundancy repair signal that indicates an address of the defective memory cell row; and

a row decoder for receiving a row address signal that indicates a memory cell row including a memory cell to be accessed and selecting the redundant memory cell row in accordance with the redundancy repair signal generated by the redundancy repair signal generator;

wherein the redundancy repair signal generator is located opposite to the row decoder with the memory cell array sandwiched between the row decoder and the redundancy repair signal generator.

2. The semiconductor memory according to claim 1, wherein a redundancy repair signal line for supplying the redundancy repair signal to the row decoder is arranged between the row decoder and the redundancy repair signal generator and extends across the memory cell array.

3. The semiconductor memory according to claim 2, further comprising a plurality of word lines arranged in the row direction for each of the memory cell rows so that the row decoder selects one row of the memory cell rows in accordance with the row address signal,

wherein the redundancy repair signal line is located between adjacent word lines of the word lines.

4. The semiconductor memory according to claim 3, wherein the redundancy repair signal line and the word lines are formed in the same wiring layer.

5. The semiconductor memory according to claim 1, wherein the semiconductor memory is formed as a static random access memory

(SRAM),

the memory cell array and the row decoder are located inside a SRAM macro, and

the redundancy repair signal generator is located outside the SRAM macro.

6. The semiconductor memory according to claim 1, wherein the row decoder selects the redundant memory cell row when the address of the memory cell row indicated by the row address signal is matched with the address of the defective memory cell row indicated by the redundancy repair signal.

7. The semiconductor memory according to claim 1, wherein the memory cell array is rectangular in shape,

the row decoder faces one side of the memory cell array in a column direction, and

the redundancy repair signal generator faces the other side of the memory cell array in the column direction.

8. The semiconductor memory according to claim 1, wherein the memory cells and the redundant memory cells are arranged in matrix form, and

the semiconductor memory further comprises a column decoder for receiving a column address signal that indicates a memory cell column including the memory cell to be accessed and selecting the memory cell column indicated by the column address signal.

9. A semiconductor memory comprising:

first and second memory cell arrays, each of which comprises a plurality of memory cell rows and at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, and the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction;

a redundancy repair signal generator for generating a redundancy repair signal that indicates an address of the defective memory cell row; and

a row decoder for receiving a row address signal that indicates a memory cell row including a memory cell to be accessed and selecting the redundant memory cell row in accordance with the redundancy repair signal generated by the redundancy repair signal generator;

wherein the row decoder is located between the first memory cell array and the second memory cell array, and

the redundancy repair signal generator is located opposite to the row decoder with the first memory cell array sandwiched between the row decoder and the redundancy repair signal generator.

10. The semiconductor memory according to claim 9, wherein a redundancy repair signal line for supplying the redundancy repair signal to the row decoder is arranged between the row decoder and the redundancy repair signal generator and extends across the first memory cell array.

11. The semiconductor memory according to claim 9, further comprising a plurality of word lines arranged in the row direction for each of the memory cell rows so that the row decoder selects one row of the memory cell rows in accordance with the row address signal,

wherein each of the word lines extends across the first memory cell array, the row decoder, and the second memory cell array.

12. A semiconductor memory comprising:

a memory cell array comprising a plurality of memory cell rows, at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, and at least one redundant memory cell column for repairing a defective memory cell column of a plurality of memory cell columns that includes the defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction, and the at least one redundant memory cell column comprising a plurality of redundant memory cells arranged in a column direction;

a first redundancy repair signal generator for generating a first redundancy repair signal that indicates an address of the defective memory cell row;

a row decoder for receiving a row address signal that indicates a

memory cell row including a memory cell to be accessed and selecting the redundant memory cell row in accordance with the first redundancy repair signal generated by the first redundancy repair signal generator;

a second redundancy repair signal generator for generating a second redundancy repair signal that indicates an address of the defective memory cell column; and

a column decoder for receiving a column address signal that indicates a memory cell column including the memory cell to be accessed and selecting the redundant memory cell column in accordance with the second redundancy repair signal generated by the second redundancy repair signal generator;

wherein the first redundancy repair signal generator is located opposite to the row decoder with the memory cell array sandwiched between the row decoder and the first redundancy repair signal generator, and

the second redundancy repair signal generator is located opposite to the column decoder with the memory cell array sandwiched between the column decoder and the second redundancy repair signal generator.

13. The semiconductor memory according to claim 12, wherein a first redundancy repair signal line for supplying the first redundancy repair signal to the row decoder is arranged between the row decoder and the first redundancy repair signal generator and extends across the memory cell array, and

a second redundancy repair signal line for supplying the second redundancy repair signal to the column decoder is arranged between the column decoder and the second redundancy repair signal generator and extends across the memory cell array.

14. The semiconductor memory according to claim 12, wherein the memory cell array is rectangular in shape,

the row decoder faces one side of the memory cell array in the column direction,

the first redundancy repair signal generator faces the other side of the memory cell array in the column direction,

the column decoder faces one side of the memory cell array in the row direction, and

the second redundancy repair signal generator faces the other side of

the memory cell array in the row direction.

15. A semiconductor memory comprising:

first, second, third, and fourth memory cell arrays, each of which comprises a plurality of memory cell rows, at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, and at least one redundant memory cell column for repairing a defective memory cell column of a plurality of memory cell columns that includes the defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction, and the at least one redundant memory cell column comprising a plurality of redundant memory cells arranged in a column direction;

first and second row redundancy repair signal generators for generating first and second row redundancy repair signals respectively, each of the first and second row redundancy repair signals indicating an address of the defective memory cell row;

first and second row decoders for receiving a row address signal that indicates a memory cell row including a memory cell to be accessed and selecting the redundant memory cell row respectively in accordance with the first and second row redundancy repair signals generated by the first and second row redundancy repair signal generators;

first and second column redundancy repair signal generators for generating first and second column redundancy repair signals respectively, each of the first and second column redundancy repair signals indicating an address of the defective memory cell column; and

first and second column decoders for receiving a column address signal that indicates a memory cell column including the memory cell to be accessed and selecting the redundant memory cell column respectively in accordance with the first and second column redundancy repair signals generated by the first and second column redundancy repair signal generators;

wherein the first row decoder is located between the first memory cell array and the second memory cell array that are arranged in the row direction,

the second row decoder is located between the third memory cell

array and the fourth memory cell array that are arranged in the row direction,

the first column decoder is located between the first memory cell array and the third memory cell array that are arranged in the column direction,

the second column decoder is located between the second memory cell array and the fourth memory cell array that are arranged in the column direction,

the first row redundancy repair signal generator is located opposite to the first row decoder with the first memory cell array sandwiched between the first row decoder and the first row redundancy repair signal generator,

the second row redundancy repair signal generator is located opposite to the second row decoder with the third memory cell array sandwiched between the second row decoder and the second row redundancy repair signal generator,

the first column redundancy repair signal generator is located opposite to the first column decoder with the first memory cell array sandwiched between the first column decoder and the first column redundancy repair signal generator, and

the second column redundancy repair signal generator is located opposite to the second column decoder with the second memory cell array sandwiched between the second column decoder and the second column redundancy repair signal generator.

16. The semiconductor memory according to claim 15, wherein a first row redundancy repair signal line for supplying the first row redundancy repair signal to the first row decoder is arranged between the first row decoder and the first row redundancy repair signal generator and extends across the first memory cell array,

a second row redundancy repair signal line for supplying the second row redundancy repair signal to the second row decoder is arranged between the second row decoder and the second row redundancy repair signal generator and extends across the third memory cell array,

a first column redundancy repair signal line for supplying the first column redundancy repair signal to the first column decoder is arranged between the first column decoder and the first column redundancy repair

signal generator and extends across the first memory cell array, and

a second column redundancy repair signal line for supplying the second column redundancy repair signal to the second column decoder is arranged between the second column decoder and the second column redundancy repair signal generator and extends across the second memory cell array.

17. A semiconductor memory comprising:

first and second memory cell arrays, each of which comprises a plurality of memory cell rows and at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, and the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction;

a first redundancy repair signal generator for generating a first redundancy repair signal that indicates an address of the defective memory cell row of the first memory cell array;

a second redundancy repair signal generator for generating a second redundancy repair signal that indicates an address of the defective memory cell row of the second memory cell array;

a first row decoder for receiving a row address signal that indicates a memory cell row including a memory cell to be accessed and selecting the redundant memory cell row of the first memory cell array in accordance with the first redundancy repair signal generated by the first redundancy repair signal generator; and

a second row decoder for receiving the row address signal and selecting the redundant memory cell row of the second memory cell array in accordance with the second redundancy repair signal generated by the second redundancy repair signal generator;

wherein the first and second redundancy repair signal generators are located between the first memory cell array and the second memory cell array,

the first row decoder is located opposite to the first redundancy repair signal generator with the first memory cell array sandwiched between the first row decoder and the first redundancy repair signal generator, and

the second row decoder is located opposite to the second redundancy repair signal generator with the second memory cell array sandwiched between the second row decoder and the second redundancy repair signal generator.

18. The semiconductor memory according to claim 17, wherein a first redundancy repair signal line for supplying the first redundancy repair signal to the first row decoder is arranged between the first row decoder and the first redundancy repair signal generator and extends across the first memory cell array, and

a second redundancy repair signal line for supplying the second redundancy repair signal to the second row decoder is arranged between the second row decoder and the second redundancy repair signal generator and extends across the second memory cell array.

19. The semiconductor memory according to claim 17, wherein the semiconductor memory is formed as a static random access memory (SRAM),

the first and second memory cell arrays and the first and second redundancy repair signal generators are located inside a SRAM macro, and

the first and second row decoders are located outside the SRAM macro.

20. A semiconductor memory comprising:

first and second memory cell arrays, each of which comprises a plurality of memory cell rows and at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, and the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction;

a redundancy repair signal generator for generating a first redundancy repair signal that indicates an address of the defective memory cell row of the first memory cell array and a second redundancy repair signal that indicates an address of the defective memory cell row of the second memory cell array;

a first row decoder for receiving a row address signal that indicates

a memory cell row including a memory cell to be accessed and selecting the redundant memory cell row of the first memory cell array in accordance with the first redundancy repair signal generated by the redundancy repair signal generator; and

a second row decoder for receiving the row address signal and selecting the redundant memory cell row of the second memory cell array in accordance with the second redundancy repair signal generated by the redundancy repair signal generator;

wherein the redundancy repair signal generator is located between the first memory cell array and the second memory cell array,

the first row decoder is located opposite to the redundancy repair signal generator with the first memory cell array sandwiched between the first row decoder and the redundancy repair signal generator, and

the second row decoder is located opposite to the redundancy repair signal generator with the second memory cell array sandwiched between the second row decoder and the redundancy repair signal generator.

21. The semiconductor memory according to claim 20, wherein a first redundancy repair signal line for supplying the first redundancy repair signal to the first row decoder is arranged between the first row decoder and the redundancy repair signal generator and extends across the first memory cell array, and

a second redundancy repair signal line for supplying the second redundancy repair signal to the second row decoder is arranged between the second row decoder and the redundancy repair signal generator and extends across the second memory cell array.

22. The semiconductor memory according to claim 20, wherein the semiconductor memory is formed as a static random access memory (SRAM),

the first and second memory cell arrays and the redundancy repair signal generator are located inside a SRAM macro, and

the first and second row decoders are located outside the SRAM macro.

23. The semiconductor memory according to claim 20, wherein the redundancy repair signal generator comprises:

a redundancy repair information memory for storing information of the first and second redundancy repair signals,

a switching means for supplying the first and second redundancy repair signals represented by the information stored in the redundancy repair information memory to the first and second row decoders, respectively; and

a switching control means for controlling operation of the switching means.

24. A semiconductor memory comprising:

first and second memory cell arrays, each of which comprises a plurality of memory cell rows and at least one redundant memory cell row for repairing a defective memory cell row of the memory cell rows that includes a defective memory cell, each of the memory cell rows comprising a plurality of memory cells arranged in a row direction, and the at least one redundant memory cell row comprising a plurality of redundant memory cells arranged in the row direction;

a redundancy repair signal generator for generating a first redundancy repair signal that indicates an address of the defective memory cell row of the first memory cell array and a second redundancy repair signal that indicates an address of the defective memory cell row of the second memory cell array;

a first row decoder for receiving a row address signal that indicates a memory cell row including a memory cell to be accessed and selecting the redundant memory cell row of the first memory cell array in accordance with the first redundancy repair signal generated by the redundancy repair signal generator; and

a second row decoder for receiving the row address signal and selecting the redundant memory cell row of the second memory cell array in accordance with the second redundancy repair signal generated by the redundancy repair signal generator;

wherein the redundancy repair signal generator is located between the first memory cell array and the second memory cell array,

the first row decoder is located between the first memory cell array and the redundancy repair signal generator, and

the second row decoder is located between the second memory cell array and the redundancy repair signal generator.

25. A semiconductor memory comprising:

first and second memory cell arrays, each of which comprises a plurality of memory cell columns and at least one redundant memory cell column for repairing a defective memory cell column of the memory cell columns that includes a defective memory cell, each of the memory cell columns comprising a plurality of memory cells arranged in a column direction, and the at least one redundant memory cell column comprising a plurality of redundant memory cells arranged in the column direction;

a redundancy repair signal generator for generating a redundancy repair signal that indicates an address of the defective memory cell column; and

a column decoder for receiving a column address signal that indicates a memory cell column including a memory cell to be accessed and selecting the redundant memory cell column in accordance with the redundancy repair signal generated by the redundancy repair signal generator;

wherein the column decoder is located between the first memory cell array and the second memory cell array, and

the redundancy repair signal generator is located opposite to the column decoder with the first memory cell array sandwiched between the column decoder and the redundancy repair signal generator.